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Hiring Manager
Re: ASIC Physical Design / Power / Timing (AI/ML-aware)

Hello Hiring Manager,

I am applying for an ASIC Physical Design role with emphasis on timing closure, power analysis, and signoff discipline. I bring 30+ years of RTL-to-GDSII delivery experience across multiple companies and advanced technology nodes, including recent work on TSMC 4nm/5nm designs using Synopsys Fusion Compiler/ICC2 and Cadence Innovus.

My strengths align with teams that need predictable closure and clean releases:

- Timing closure and STA/MMMC using PrimeTime (WNS/TNS, clock-path optimization, constraint quality).
- Vector-based and RTL-aware power analysis using PrimePower/PT-PX (VCD/FSDB activity correlation; post-layout parasitics).
- Low-power UPF implementation (multi-domain, isolation, retention, level shifters, power-state verification).
- Automation in Python/Tcl to reduce iteration time and standardize signoff packages.

In parallel, I am strengthening ML/AI capabilities through eCornell coursework and hands-on projects focused on practical automation for EDA workflows—targeting faster convergence, improved reporting, and repeatable decision-making.

I would welcome the opportunity to discuss your current design challenges and how I can contribute immediately. My resume is attached for review.

Sincerely,

Ruben Reyes