Ruben Reyes

Sunnyvale, California | Email: Ruben.Reyes@AthenaCloudEngineers.com | Telephone: (408) 857 - 4771

ASIC Physical Design / ML-AI Engineer

PROFESSIONAL SUMMARY

Seasoned ASIC Physical Design Engineer with a Master's in Electrical Engineering and over 30 years of experience in high-speed ASIC design, SoC integration, and advanced R&D in physics. Successfully completed 19+ tape-outs across multiple companies and process nodes, adept at managing multi-million gate designs from RTL to GDS using industry-standard EDA tools such as Synopsys IC Compiler (ICC2), Cadence Innovus, and PrimeTime PX/SI. Demonstrated hands-on expertise in logic synthesis, timing closure, DFT techniques, power optimization, and customized P&R flows for advanced process nodes down to 4nm.

Currently enhancing expertise in Machine Learning & AI through eCornell's ML/AI Certification Program, focusing on supervised learning, deep learning, NLP, and AI-driven automation. Skilled in data preprocessing, feature engineering, model training, and performance evaluation using industry-standard tools such as Python, NumPy, Pandas, Scikit-learn, and Jupyter Notebooks. Passionate about leveraging ML-driven automation for ASIC/EDA workflows, improving timing closure, power analysis, and predictive modeling for enhanced semiconductor design efficiencies.

Recognized for strong leadership, problem-solving, and cross-functional collaboration, with a proven track record of coordinating global teams and delivering innovative solutions under tight deadlines. Adept at scripting and automation (Python, Tcl, Shell, SED, AWK) to drive efficiency in design methodologies.

SKILLS

Scripting Languages: SED, Awk, UNIX, Tcl, Python, C, Pascal, FORTRAN, Assembler, BASIC
Methodologies: RTL to tapeout GDS, SIEMENS tapeout design flow, INFINEON design flow, Synopsys RM tapeout flow, Cadence design flow, low power methodology, TSMC Reference Flow 4.0, custom RTL-to-GDS flow.
Designs: Custom CPU (IBM PowerPC), DDR PHY, graphic chips, voice recognition IP, VP9 codec, CPU, SAOC, register, GDDR, RFID, H.264 codec, PCIX, several test chips.
Machine Learning/AI: ChatGPT, Gemini, Croq/X, Microsoft Copilot, Kaggle, GitHub, Hugging Face, Ollama, Colab, Jupyter Lab
EDA Tools: RTL Architect, Fusion Compiler, RedHawk, Xcelium, PrimePower, Verdi, ICC2, Innovus, PrimeTime-PX, VCLP, C, Shell, Makefile, Star-RCXT, LEF/DEF, Tcl, IC Validator/VUE, PrimeTime-SI, Virtuoso, RedHawk (ALP), Calibre, FlowTracer, CVS, Perforce, ClearCase, GIT, LSF, Design Compiler, Conformal, Formality, Voltus, Tempus, Genus, First Encounter XL, SKILL programming, Place & Route, Silicon Ensemble, Cell3, Preview, CTGEN, Dracula, DIVA, Layout Editor, Pcells, Arcadia, FlexRoute, Chip Architect, Astro, Wroute, IBM Niagara, Apollo, IBM BullDozer, PEARL.
Process: TSMC down to 4nm, Samsung down to 20nm, Chartered down to 20nm, Intel down to 20nm, UMC down to 20nm, GlobalFoundries down to 20nm, IBM down to 250nm
ASIC Libraries: TSMC 90nm down to 4nm, GlobalFoundries 20nm, Samsung 20nm, IBM CMOS7X 250nm

PERMAMENT/CONSULTANT WORK EXPERIENCE

Athena Cloud Engineers, LLC | Sunnyvale, CA
Principal ASIC Physical Design Engineer | Sept 2024 – DATE

- Led **RTL-to-GDSII ASIC physical design and signoff** for **AI/ML compute workloads**, driving **PPA optimization** across **advanced technology nodes** using **Fusion Compiler, ICC2, and Innovus**.
- Achieved **timing closure** through **PrimeTime STA**, resolving **WNS/TNS**, **clock-path optimization**, and **MMMC constraints** on complex AI accelerator designs.
- Executed **RTL-aware and vector-based power analysis** with **PrimePower**, correlating **VCD/FSDB activity** and **post-layout parasitics** to improve **dynamic and leakage power accuracy**.
- Implemented **low-power architectures** using **UPF**, including **multi-power domains**, **isolation**, **retention**, **level shifters**, and **power-state verification**.
- Integrated **physical design signoff expertise** with **AI-aware compute requirements**, maintaining **strict NDA compliance**, and reinforced alignment through **graduate-level AI/ML coursework (eCornell)** applied to **EDA optimization workflows**.

META | Sunnyvale, CA
ASIC Physical Design Engineer and ASIC Power Engineer (Contract) | Sept 2022 – Sept 2024

- Evaluated **RTL architecture for low-power design**, focusing on **timing paths, power, and area** optimization.
- Developed **Tcl and Python scripts** for **power analysis and optimization**.
- Led **multi-team collaboration**, managing project documentation and progress tracking in **Google Docs**.

- Utilized **Cadence Innovus and Synopsys Fusion Compiler** on **TSMC 4nm designs**.
- Debugged **UPF files, SDC constraints, routing congestion, IR/EM issues** using **RedHawk and PNR tools**.
- Authored **internal documentation** on **power optimization and PNR methodologies**.

MAXENTRIC | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Jan 2021 – Sept 2022

- Collaborated with **India PD team** to resolve **physical design and static timing** challenges near **tape-out**.
- Delivered **alternative solutions for SDC clock issues** and created **Structured Design Placement (SDP) files**.
- Assessed **bottom-up timing constraints** using **Cadence Tempus and Genus**.

GOOGLE | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Feb 2021 – Feb 2022

- Conducted **power analysis using PrimePower** on **TSMC 5nm designs**.
- Integrated **Xtensa compiler and Xcelium** to extract power data for analysis.
- Automated workflows using **Bash scripting and FlowTracer**.

MICROSOFT | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Jan 2021 – Jun 2021

- Led **timing constraint fixes and STA analysis** on **TSMC 5nm blocks** using **Cadence Innovus**.
- Used **PrimeTime and PT-PX for power analysis**, **Voltus for rail analysis**, and **Calibre for DRC/LVS**.
- Automated portions of the **design flow with Tcl scripts**.

SYNOPSYS | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Feb 2021 – Jul 2021

- Led **tape-out using Synopsys RTL2GDS flow** on **DDR5 designs** at **5nm**.
- Conducted **timing and constraint analysis, EMIR verification, and DRC/LVS fixes**.

BROADCOM | Sunnyvale, CA
ASIC Power Engineer (Contract) | Dec 2020 – Jun 2021

- Developed **UPF power intent files** and automated **power analysis workflows using Tcl and SQLite**.
- Conducted **power analysis with PrimeTime-PX and RedHawk**.

ESPERANTO TECHNOLOGIES | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Jan 2019 – Dec 2019

- Worked on **block-level NOC chip (26M gates, 1 GHz, TSMC 7nm)**, optimizing **UPF, timing, and floorplanning**.

ASTERA LABS | Sunnyvale, CA
ASIC Physical Design Verification Engineer (Contract) | Jan 2019 – Mar 2019

- Performed **full-chip DRC/LVS/ANT/DFM analysis and repairs** for **tape-out**.

INTEL | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Apr 2016 – Dec 2018

- Led **DRC/LVS debugging** for **Intel 10nm** technology using **Synopsys ICV and RVE**.
- Created **Makefile automation** for repetitive design rule checks and fixes.
- Designed **custom power/ground rail grids** and assisted in **floorplanning, timing convergence, and design flow integration**.

QUALCOMM | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Sept 2016 – Dec 2016

- Delivered **netlist-to-GDSII** for **180nm TSMC mixed-signal VLSI designs**.
- Performed **timing convergence and constraint optimizations using PrimeTime**.

GOOGLE | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Mar 2015 – Jun 2016

- Led **floorplanning and timing closure** for **VP9 encoder/decoder (16nm, TSMC)**.
- Optimized **6 blocks (7M gates each)** to achieve **negative slack reduction below 100ps**.

BROADCOM | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Nov 2015 – Jan 2016

- Conducted **full-chip static timing analysis** under **tight tape-out deadlines**.
- Wrote **Tcl scripts for automated timing report parsing**.

PNY TECHNOLOGIES | San Jose, CA
ASIC Physical Design Engineer (Contract) | Jan 2015 – Nov 2015

- Evaluated **Cadence/Synopsys tool suites** for **SSD controller design flows**.

AMD | Sunnyvale, CA
Member of Technical Staff | Jul 2012 – Oct 2014

- Led **timing closure, power integrity, and RedHawk ALP analysis** for **TSMC 32nm/28nm and GlobalFoundries 28nm/20nm**.
- Developed **EDA methodology enhancements and custom automation scripts**.

AMD | Sunnyvale, CA
ASIC Physical Design Engineer (Contract) | Sept 2011 – Jul 2012

- Led **PCIE design implementation** in **GDDR-based SoC** using **ICC1 and Synopsys tools**.
- Developed **low-power UPF methodologies** and implemented **DFT scan chains**.

EARLY CAREER EXPERIENCE (1982 – 2009)

Synapse, Inc. | Sunnyvale, CA
ASIC Physical Design Engineer | Jun 2010 – Sept 2011

- Executed **place-and-route** for high-performance designs using **Cadence/Synopsys flows**; optimized **timing and power** across multiple corners, ensuring successful **tape-out**.

Chipstart, LLC | Palo Alto, CA
Design Business Manager | Dec 2009 – Jun 2010

- Served as a **technical liaison** between **sales, marketing, and engineering** for ASIC IP deployment; managed **customer deliverables**, aligning **technical solutions with business objectives**.

Trivium Tech Force Corp. & Global Trivium Corp. | Sunnyvale, CA
ASIC Design Manager | Jun 2008 – Dec 2009

- Led **cross-functional teams**, managing **multi-site schedules and resource allocations** for ASIC projects; implemented **risk management and design reviews** to maintain project milestones.

QThink, Inc. | San Jose, CA
ASIC Physical Design Engineer | Jan 2004 – Jan 2008

- Executed **netlist-to-GDS** for **consumer electronics SoCs**, ensuring **DRC/LVS sign-off** under tight schedules; used **Cadence Encounter** for **floorplanning, timing closure, and route optimization**.

Arrow Electronics, Inc. | Woodland Hills, CA
ASIC Physical Design Consultant | Sept 2003 – Jan 2004

- Provided **consultancy for semiconductor design**, optimizing **timing, power, and area**; mentored **junior engineers** on **DRC, LVS, and industry-standard EDA flows**.

Synopsys, Inc. | Mountain View, CA
ASIC Physical Design Engineer | Aug 1998 – Sept 2003

- Supported **customer engagements** in **Design Compiler, PrimeTime**, and other **Synopsys tools**; refined **reference flows for advanced nodes (90nm, 65nm)** and guided teams on **RTL-to-GDS** best practices.

Cadence Design Systems, Inc. | San Jose, CA
ASIC Physical Design Engineer | Sept 1996 – Aug 1998

- Led **place-and-route solutions** for **high-speed and low-power designs** using **Cadence tool suites**; developed **custom SKILL scripts** to **automate design tasks**, reducing **P&R cycle times by ~20%**.

IBM, Inc. | Yorktown Heights, NY
Engineer | Dec 1982 – Jan 1996

- Conducted **R&D in advanced CMOS processes**, collaborating on **microprocessor design**; authored and **co-authored patents**, driving **ASIC methodology advancements**.

EDUCATION

- Master of Science in Electrical Engineering – Polytechnic University, Brooklyn, New York, 1995
- Bachelor of Science in Electrical Engineering with Honors – Pratt Institute, Brooklyn, New York, 1991

CERTIFICATIONS

- IBM Research, Columbia, Cornell, MIT – All their EDA tool training and updates, Custom Integrated Design Training Program
- Cornell – Applied Machine Learning and AI (in progress), Python Programming
- Synopsys – Project Manager, All their EDA tool training and updates
- DeAnza College – Business Supervisory Management, Business Management
- Project Management Institute IP – Project Management Program
- Avanti – All their EDA tool training and updates
- Cadence – All their EDA tool training and updates
- Cooper & Chyan Technology – IC Craftsman
- MAGMA – All their EDA tool training and updates

EXTRACURRICULAR ACTIVITIES

- IBM Research, IBM patents
- Synopsys, Cadence, Tau Beta Pi, IEEE
- Eta Kappa Nu (President)
- Pratt Institute Trustee & Chairman
- IBM patents/publications
- Global Trivium Corp., Athena Cloud Engineers, LLC.
- Authored technical papers

- Recognized for technical contributions to IBM products